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**[4757]-1088**

**S.E. (Information Technology) (Second Semester) EXAMINATION, 2015**

**PROCESSOR ARCHITECTURE AND INTERFACING**

**(2012 PATTERN)**

**Time : Two Hours**

**Maximum Marks : 50**

**N.B. :—** (i) Attempt Q. No. 1 or Q. No. 2, Q. No. 3 or Q. No. 4,  
Q. No. 5 or Q. No. 6, Q. No. 7 or Q. No. 8

(ii) Neat diagrams must be drawn wherever necessary.

(iii) Draw the figures to the right indicate full marks.

(iv) Assume suitable data, if necessary.

1. (a) Differentiate between procedure and macro. [6]

(b) Explain difference between 80386 pipelined and non-pipelined bus cycle with neat diagram. [6]

*Or*

2. (a) Explain the following assembler directives :

(i) Public and Extern

(ii) .Org

(iii) : Model [6]

P.T.O.

- (b) State and explain the significance of any *three* interrupt related signals of the 80386. [6]
3. (a) Draw and explain the logical address to physical address translation with paging in 80386 processor. [6]
- (b) What is virtual mode ? How to switch from protected mode to virtual 86 mode. [6]

*Or*

4. (a) Write down the steps to switch from Real Mode (RM) to Protected Mode (PM). [6]
- (b) Explain the difference between 3 operating models of 80386. [6]
5. (a) Identify and justify addressing mode of the following 8051 instructions : [6]
- (i) MOV @ RO, A
- (ii) MOV B, 50H
- (iii) DIV AB.
- (b) List SFR's used in 8051. Draw and explain SCON and TCON. [7]

*Or*

6. (a) Explain the following instructions in 8051 : [6]
- (i) MUL AB
  - (ii) SWAP A
  - (iii) MOV DPTR, #3000H
- (b) List the features of 8051 microcontroller. Draw and explain architecture of 8051. [7]
7. (a) How many interrupts are there in 8051 ? List them according to their priority. Explain the IP register structure. [7]
- (b) Explain any *two* operating modes of timer used in 8051. [7]

*Or*

8. (a) List and classify 8051 interrupts. [7]
- (b) Draw and explain formats of SBUF and IE. [6]